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1 Binary synthesis

Greg Stitt, Frank Vahid

August 2007 **Transactions on Design Automation of Electronic Systems****Publisher:** ACMFull text available: Pdf (341.48 KB) [Additional Information: full citation, abstract, re](#)**Bibliometrics:** Downloads (6 Weeks): 24, Downloads (12 Months): 174, Citation

Recent high-level synthesis approaches and C-based hardware description languages improve the hardware design process by allowing developers to capture functionality in a well-known high-level source language. However, these

Keywords: Binary synthesis, FPGA, configurable logic, hardware/software partitioning, synthesis from software binaries, warp

2 Synthesis of Heterogeneous Distributed Architectures for Memory-In

Chao Huang, Sriyaths Ravi, Anand Raghunathan, Niraj K. Jha
 November 2003 **ICCAD '03: Proceedings of the 2003 IEEE/ACM International Conference on Computer-Aided Design**

Publisher: IEEE Computer SocietyFull text available: Pdf (756.95 KB) [Additional Information: full citation, abstract, re](#)**Bibliometrics:** Downloads (6 Weeks): 5, Downloads (12 Months): 26, Citation (

Memory-intensive applications present unique challenges to an ASIC designer. Memory organization, memory size requirements, bandwidth and access latency are critical to the performance of single-chip distributed logic-memory architectures ...

3 Inter-cluster communication in VLIW architectures

A. S. Terezhko, H. Corporaal

June 2007 **Transactions on Architecture and Code Optimization (TACO)****Publisher:** ACMFull text available: Pdf (996.47 KB) [Additional Information: full citation, abstract, re](#)**Bibliometrics:** Downloads (6 Weeks): 24, Downloads (12 Months): 162, Citation

The traditional VLIW (very long instruction word) architecture with a single scale up well to address growing performance demands on embedded processors. Splitting a VLIW processor in smaller clusters, which are ...

Keywords: Instruction-level parallelism, VLIW, clock frequency, cluster scheduler, intercluster communication, optimizing compiler, pipelining, i

4 [An embedded system case study: the firm ware development envirc](#)
[audio processor](#)



Clifford Liem, Marco Cornero, Miguel Santana, Pierre Paulin, Ahmed Jerray, Lopez, Xavier Figari, Laurent Bergher

June 1997 **DAC '97**: Proceedings of the 34th annual conference on Design

Publisher: ACM

Full text available: Pdf (52.50 KB)

Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 23, Citation (

This paper outlines a case study at SGS-Thomson Microelectronics on the development environment in co-operation with Thomson Consumer Electronics. The environment is for an embedded processor used for audio decompression.

5 [Architecture description language \(ADL\)-driven software toolkit gene](#)
[exploration of programmable SOC's](#)



Prabhat Mishra, Aviral Shrivastava, Nikil Dutt

July 2006 **DAC '04**: Proceedings of the 41st annual conference on Design

Publisher: ACM

Full text available: Pdf (1.07 MB)

Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 16, Downloads (12 Months): 134, Citation

Advances in semiconductor technology permit increasingly complex application programmable systems-on-chips (SOCs). Furthermore, shrinking time-to-market with the need for product versioning through software modification ...

Keywords: Architecture description language, design space exploration, programmable architecture, retargetable compilation

Also published in:

July 2006 **Transactions on Design Automation of Electronic Systems (TOD**

6 [Hardware/Software Design Space Exploration for a Reconfigurable F](#)

Alberto La Rosa, Luciano Lavagno, Claudio Passerone

March 2003 **DATE '03: Proceedings of the conference on Design, Auto**

Europe - Volume 1, Volume 1

Publisher: IEEE Computer Society

Full text available: Publisher Site, Pdf (103.11 KB) Additional Information: [full citation](#), [index term](#)

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 25, Citation (

This paper describes an approach to hardware/software design space exploration for processors. The existing compiler tool-chain, because of the user-defined extended in order to offer developers an easy way ...

7 [Proceedings of the 2009 Conference on Asia and South Pacific Desi](#)
[Kazutoshi Wakabayashi](#)

January 2009 **ASP-DAC '09**: Proceedings of the 2009 Conference on Asia a
Automation


Publisher: IEEE Press

Additional Information: [full citation](#), [abstract](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citatio

On behalf of the Organizing Committee, I would like to invite you to att
Pacific Design Automation Conference 2009 (ASP-DAC 2009), being hel
Japan, from January 19 through 22, 2009, jointly with the Electronic ...

8 [An FPGA-based VLIW processor with custom hardware execution](#)

 Alex K. Jones, Raymond Hoare, Dara Kusic, Joshua Fazekas, John Foster

February 2005 **FPGA '05**: Proceedings of the 2005 ACM/SIGDA 13th interna
programmable gate arrays

Publisher: ACM

Full text available:  Pdf (220.52 KB)

Additional Information: [full citation](#), [abstract](#), [re
review](#)

Bibliometrics: Downloads (6 Weeks): 14, Downloads (12 Months): 152, Citatio

The capability and heterogeneity of new FPGA (Field Programmable Gat
to increase with each new line of devices. Efficiently programming these
difficulty. However, FPGAs continue to be utilized for algorithms ...


Keywords: NIOS, VLIW, compiler, kernels, parallelism, synthesis

9 [A system for synthesizing optimized FPGA hardware from MATLAB](#)

Malay Haldar, Anshuman Nayak, Alok Choudhary, Prith Banerjee

November 2001 **ICCAD '01**: Proceedings of the 2001 IEEE/ACM internation
aided design

Publisher: IEEE Press


Full text available:  Pdf (158.74 KB)

Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 63, Citation


Efficient high level design tools that can map behavioral descriptions to
of the key requirements to fully leverage FPGA for high throughput com
market pressures. We present a compiler that takes as ...

10 [Design and Implementation of the AEGIS Single-Chip Secure Proce: Random Functions](#)

 G. Edward Sun, Charles W. O'Donnell, Ishan Sachdev, Srinivas Devadas

June 2005 **ISCA '05**: Proceedings of the 32nd annual international sympos
Architecture

Publisher: ACM

Full text available:  Pdf (288.96 KB)

Additional Information: [full citation](#), [abstract](#), [re](#)


Bibliometrics: Downloads (6 Weeks): 29, Downloads (12 Months): 135, Citatio

Secure processors enable new applications by ensuring private and auth
even in the face of physical attack. In this paper we present the AEGIS
architecture, and evaluate its RTL implementation on FPGAs. By using ..

Also published in:


May 2005 **SIGARCH Computer Architecture News** Volume 33 Issue 2

11 Improving Program Efficiency by Packing Instructions into Registers

 Stephen Hines, Joshua Green, Gary Tyson, David Whalley

June 2005 **ISCA '05: Proceedings of the 32nd annual international symposium on Computer Architecture**

Publisher: ACM

Full text available:  Pdf (316.46 KB)

[Additional Information: full citation, abstract, re](#)


Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 54, Citation (

New processors, both embedded and general purpose, often have confl involving space, power, and performance. Architectural features and co target one or more design goals at the expense of the others. ...

Also published in:


May 2005 **SIGARCH Computer Architecture News** Volume 33 Issue 2

12 The WaveScalar architecture

 Steven Swanson, Andrew Schwerin, Martha Mercialdi, Andrew Petersen, An Michelson, Mark Oskin, Susan J. Eggers

May 2007 **Transactions on Computer Systems (TOCS)**, Volume 25 Issue

Publisher: ACM

Full text available:  Pdf (898.53 KB)

[Additional Information: full citation, abstract, re](#)

Bibliometrics: Downloads (6 Weeks): 26, Downloads (12 Months): 208, Citatio

Silicon technology will continue to provide an exponential increase in th transistors. Effectively translating this resource into application perform challenge that conventional superscalar designs will not ...


Keywords: WaveScalar, dataflow computing, multithreading

13 ASIP instruction encoding for energy and area reduction

 Paul Morgan, Richard Taylor

June 2007 **DAC '07: Proceedings of the 44th annual conference on Design Automation**

Publisher: ACM

Full text available:  Pdf (201.79 KB)

[Additional Information: full citation, abstract, re](#)

Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 30, Citation (

Application-specific VLIW processors provide an energy and area efficien performance embedded applications. One significant design issue is tha required to express the instruction parallelism represents a ...



Keywords: ASIP, cache, cache optimization, embedded applications, ei

14 Using C based logic synthesis to bridge the productivity gap

Chris Sullivan, Alex Wilson, Stephen Chappell


January 2004 **ASP-DAC '04: Proceedings of the 2004 conference on Asia S automation: electronic design and solution fair**

Publisher: IEEE Press

Full text available:  [Publisher Site](#) ,  [Pdf \(375.82 KB\)](#) Additional Information: [full citation](#)

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 12, Citation (

Digital circuits from software designs and formal executable specification synthesized using hardware compilation or 'C based logic synthesis'. De that same formal specification and coupled with the increasing ...

- 15 [REDEFIS: a system with a redefinable instruction set processor](#)
 Victor M. GOULART FERREIRA, Lovic GAUTHIER, Takayuki KANDO, Takuma HASHINAGA, Kazuaki MURAKAMI

August 2006 **SBCCI '06: Proceedings of the 19th annual symposium on Int design**


Publisher: ACM

Full text available:  [Pdf \(930.50 KB\)](#) Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 23, Citation (

The growing complexity and production cost of processor-based system constraints in SoC design of new systems. GPPs and ASICs are unable to power constraints, or too complex to design in short TAT/TTM. REDEFIS

Keywords: ISA customization, SoC, dynamically reconfigurable processor power

- 16 [Behavioral synthesis techniques for intellectual property protection](#)
 Farinaz Koushanfar, Inki Hong, Miodrag Potkonjak

July 2005 **Transactions on Design Automation of Electronic Systems**


Publisher: ACM

Full text available:  [Pdf \(439.81 KB\)](#) Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 40, Downloads (12 Months): 276, Citation (


We introduce dynamic watermarking techniques for protecting the value CAD and compilation tools and reusable design components. The essence the addition of a set of design and timing constraints which ...

Keywords: Intellectual property protection, behavioral synthesis, watermark

- 17 [Compiler-directed high-level energy estimation and optimization](#)
 L. Kadayil, M. Kandemir, G. Chen, N. Vijaykrishnan, M. J. Irwin, A. Sivasubramanian

November 2005 **Transactions on Embedded Computing Systems (TECS)**

Publisher: ACM

Full text available:  [Pdf \(891.31 KB\)](#) Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 20, Downloads (12 Months): 119, Citation (

The demand for high-performance architectures and powerful battery-powered systems has accentuated the need for power optimization. While many power-oriented techniques have been proposed and incorporated in current systems, ...

Keywords: Energy-Aware Compilation (EAC), mobile devices

- 18 [NoCEE: energy macro-model extraction methodology for network on chip](#)
J. Chan, S. Parameswaran
May 2005 **ICCAD '05: Proceedings of the 2005 IEEE/ACM International conference on integrated circuit design**

Publisher: IEEE Computer Society

Full text available:  Pdf (290.33 KB)


Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 9, Downloads (12 Months): 54, Citation (

In this paper we present NoCEE, a fast and accurate method for extract packet-switched network on chip (NoC) routers. Linear regression is used between events occurring in the NoC and energy consumption. ...

- 19 [Optimized Generation of Data-Path from C Codes for FPGAs](#)
Zhi Guo, Betül Büyükkurt, Walid Najjar, Kees Visser
March 2005 **DATE '05: Proceedings of the conference on Design, Automation and Test in Europe - Volume 1**, Volume 1


Publisher: IEEE Computer Society

Full text available:  Pdf (281.78 KB)

Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 52, Citation (

FPGAs, as computing devices, offer significant speedup over microprocessor configurability offers an advantage over traditional ASICs. However, the level language programmability, as microprocessors do. This ...

- 20 [Design of a SPDIF receiver using protocol compiler](#)
 Ulrich Holtmann, Peter Blinzer
May 1998 **DAC '98: Proceedings of the 35th annual conference on Design Automation Conference**

Publisher: ACM

Full text available:  Pdf (348.72 KB)

Additional Information: [full citation](#), [abstract](#), [re](#)

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 14, Citation (

This paper describes the design of a receiver for the digital audio signal players. The design was done with Protocol Compiler, a high-level synthesized structured data stream processing controllers. Compared ...

Keywords: high-level synthesis, telecommunication

Result 6

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